Sub a1

WHAT IS CLAIMED IS:

1. An image processing apparatus comprising:

an arithmetic processing unit which processes image data, being a digital signal prepared based on an image, as a manifest image, said arithmetic processing unit including,

an arithmetic processing section of SIMD (Single Instruction Multiple Data stream) type that can process a plurality of image data at the same time;

a plurality of memories connected to said arithmetic processing section; and

a memory controller which controls each of said memories,

wherein said memory controller controls transfer of image data performed between said memory and said arithmetic processing section.

2. The image processing apparatus according to claim 1, wherein said memory controller is connected to a control register, and said control register has a data transfer mode setting function for setting the data transfer mode of the memory connected to the memory controller.

3. The image processing apparatus according to claim 2, wherein said controller register changes over setting of a random access mode in which an address is set to access the memory, and setting of an automatic access mode in which an address is automatically updated to access the memory, in accordance with a control signal provided from outside.

4. The image processing apparatus according to claim 2, wherein said control register reads data redundantly from said memory, in accordance with a control signal provided from outside, and sets a redundant readout transfer mode for transferring data to said arithmetic processing section.

5. The image processing apparatus according to claim 2, wherein said control register reads data from said arithmetic processing section by thinning out, in accordance with a control signal provided from outside, and sets a thinning-out read transfer mode for transferring data to said memory.

6. An image processing apparatus comprising:

an arithmetic processing means for processing image data, being a digital signal prepared based on an image, as a manifest image, said arithmetic processing means including,

an arithmetic processing section of SIMD (Single

Instruction Multiple Data stream) type that can process a plurality of image data at the same time;

a plurality of memories connected to said arithmetic processing section; and

a memory controller for controlling each of said memories,

wherein said memory controller controls transfer of image data performed between said memory and said arithmetic processing section.

7. The image processing apparatus according to claim 6, wherein said memory controller is connected to a control register, and said control register has a data transfer mode setting function for setting the data transfer mode of the memory connected to the memory controller.

8. The image processing apparatus according to claim 7, wherein said controller register changes over setting of a random access mode in which an address is set to access the memory, and setting of an automatic access mode in which an address is automatically updated to access the memory, in accordance with a control signal provided from outside.

9. The image processing apparatus according to claim 7, wherein said control register reads data redundantly from said memory, in accordance with a control signal provided from outside, and sets a redundant readout transfer mode for transferring data to said arithmetic processing section.

10. The image processing apparatus according to claim 7, wherein said control register reads data from said arithmetic processing section by thinning out, in accordance with a control signal provided from outside, and sets a thinning-out read transfer mode for transferring data to said memory.

11. An image processing method to be executed by an image processing apparatus, said image processing apparatus including an SIMD type arithmetic processing section for processing a plurality of image data, being digital signals prepared based on an image, at the same time; a plurality of memories connected to said arithmetic processing section; and a memory controller for controlling each of said memories, the method comprising:

an image data control step for controlling transfer of image data, performed between said memory and said arithmetic processing section, by said memory controller.

12. The image processing method according to claim 11, wherein said image data control step includes a data transfer mode setting step for setting data transfer mode of memories connected to the memory controller.

13. The image processing method according to claim 11, wherein said image data control step is for changing over setting of a random access mode in which an address is set to access the memory, and setting of an automatic access mode in which an address is automatically updated to access the memory, in accordance with a control signal provided from outside.

14. The image processing method according to claim 11, wherein said image data control step is for reading data redundantly from said memory, in accordance with a control signal provided from outside, and setting a redundant readout transfer mode for transferring the data to said arithmetic processing section.

15. The image processing method according to claim 11, wherein said image data control step is for reading data from said arithmetic processing section by thinning out, in accordance with a control signal provided from outside, and setting a thinning-out read transfer mode for

transferring the data to said memory.

16. A computer readable medium for storing instructions, which when executed by a computer, causes the computer to perform an image processing method to be executed by an image processing apparatus, said image processing apparatus including an SIMD type arithmetic processing section for processing a plurality of image data, being digital signals prepared based on an image, at the same time; a plurality of memories connected to said arithmetic processing section; and a memory controller for controlling each of said memories, the method comprising:

an image data control step for controlling transfer of image data, performed between said memory and said arithmetic processing section, by said memory controller.